

# DATA SHEET

## **BLF147** VHF power MOS transistor

Product specification

September 1992

# VHF power MOS transistor

# BLF147

## FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

## DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage ( $V_{GS}$ ) information is provided for matched pair applications. Refer to 'General' section for further information.

## PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

## PIN CONFIGURATION

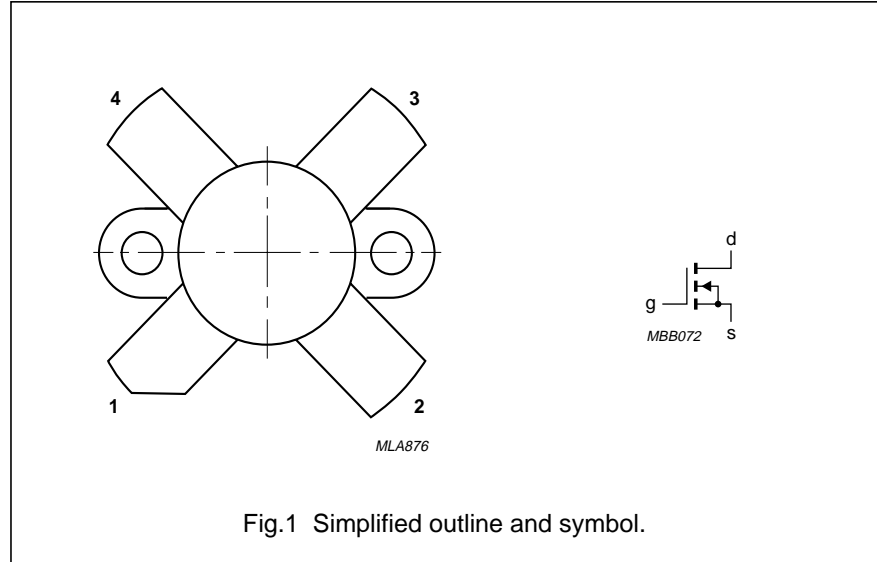


Fig.1 Simplified outline and symbol.

## CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## WARNING

**Product and environmental safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ }^\circ\text{C}$  in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_3$ (dB)	$d_5$ (dB)
SSB, class-AB	28	28	150 (PEP)	> 17	> 35	< -30	< -30
CW, class-B	108	28	150	typ. 70	typ. 70	-	-

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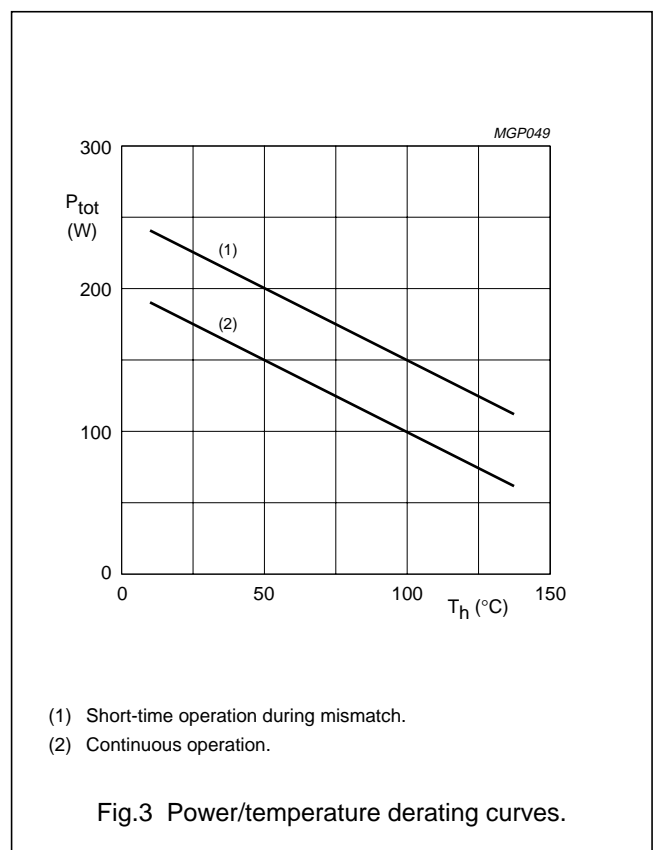
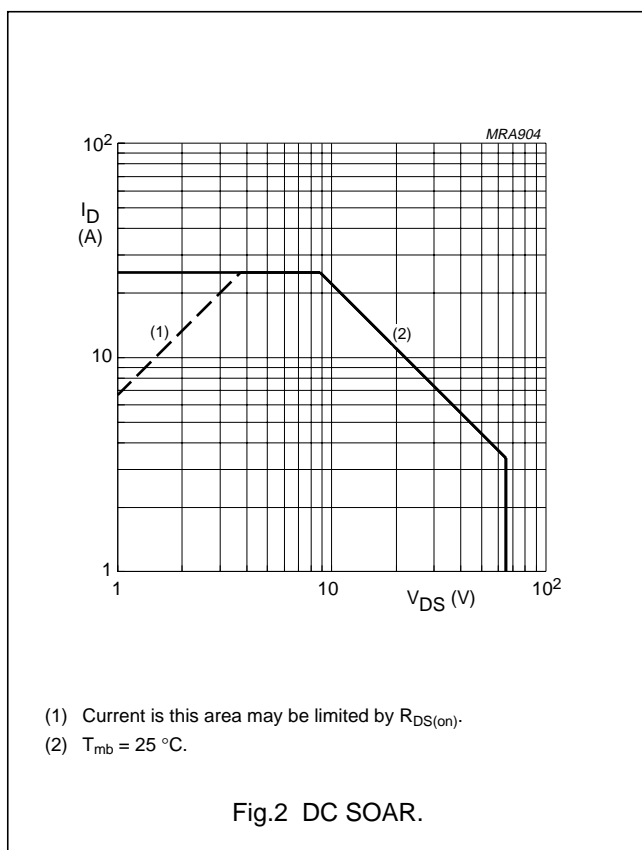
**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
$I_D$	DC drain current		–	25	A
$P_{tot}$	total power dissipation	up to $T_{mb} = 25\text{ }^\circ\text{C}$	–	220	W
$T_{stg}$	storage temperature		–65	150	$^\circ\text{C}$
$T_j$	junction temperature		–	200	$^\circ\text{C}$

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	0.8 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	0.2 K/W



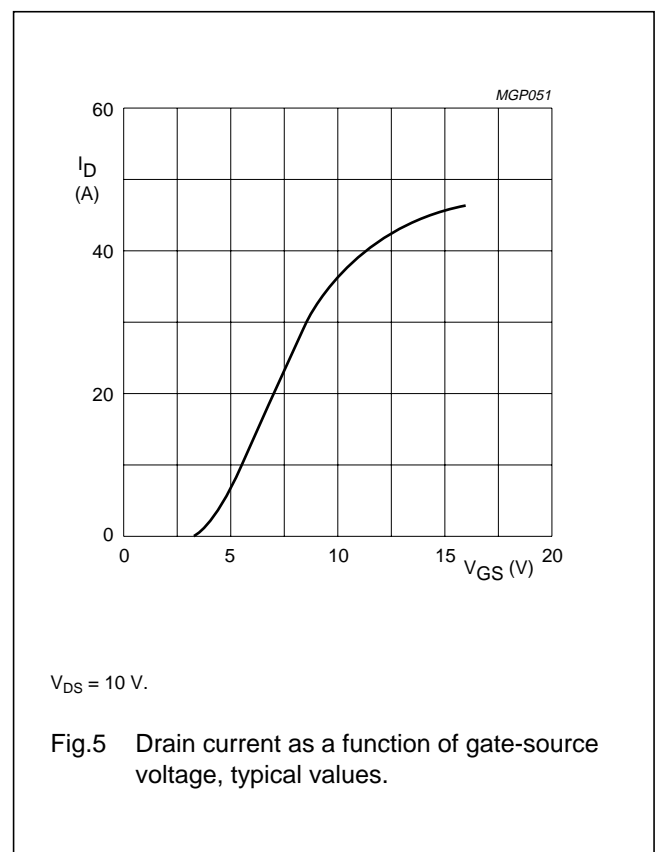
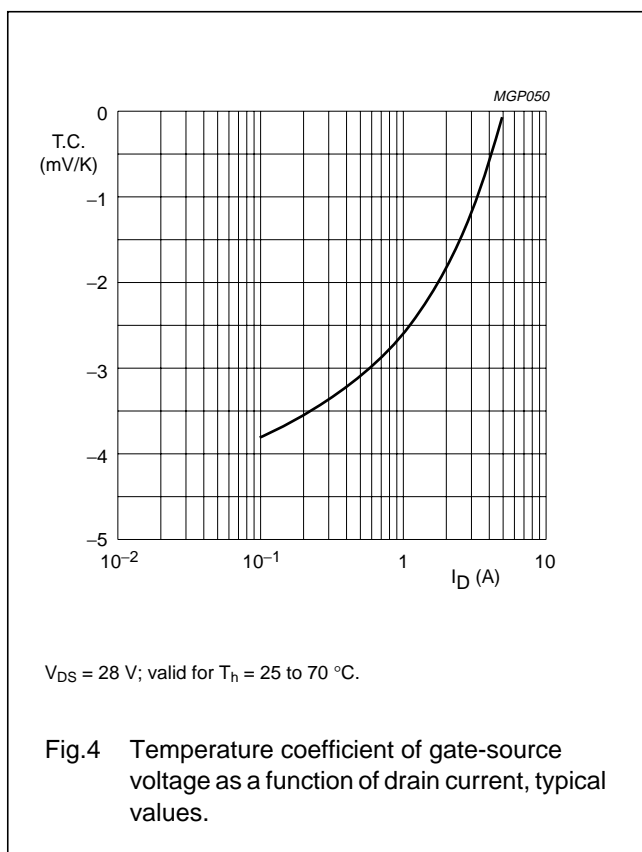
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**CHARACTERISTICS**

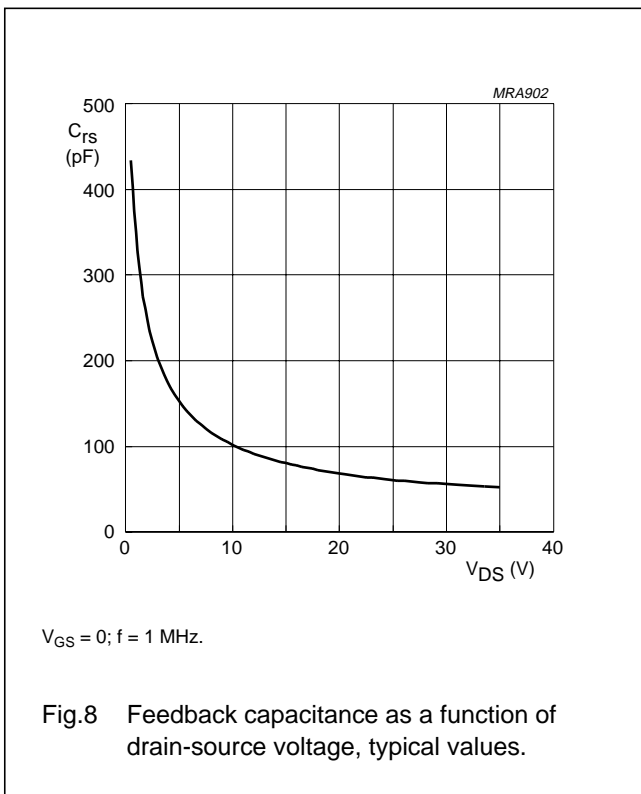
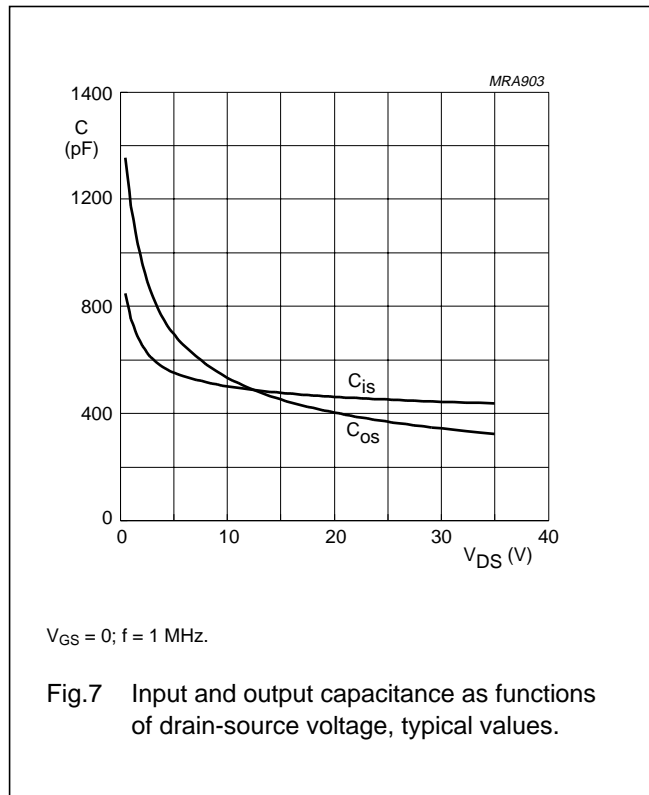
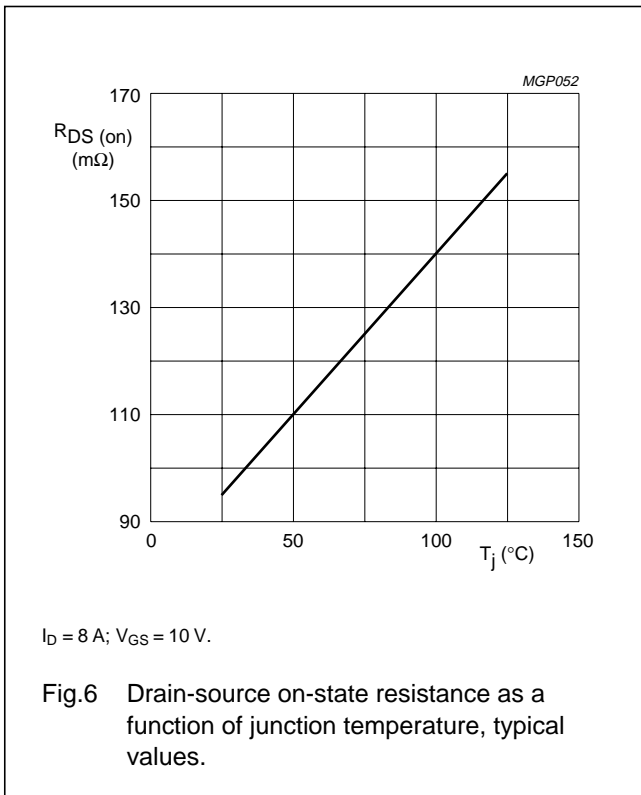
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100\text{ mA}; V_{GS} = 0$	65	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	5	mA
$I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	1	$\mu\text{A}$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 200\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
$\Delta V_{GS}$	gate-source voltage difference of matched pairs	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
$g_{fs}$	forward transconductance	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	5	7.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 8\text{ A}; V_{GS} = 10\text{ V}$	–	0.1	0.15	$\Omega$
$I_{DSX}$	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	37	–	A
$C_{is}$	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	450	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	360	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	55	–	pF



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**APPLICATION INFORMATION FOR CLASS-AB OPERATION**

$T_h = 25\text{ }^\circ\text{C}$ ;  $R_{th\text{ mb-h}} = 0.2\text{ K/W}$ ;  $R_{GS} = 9.8\text{ }\Omega$ ; unless otherwise specified.  
 RF performance in SSB operation in a common source class-AB circuit.  
 $f_1 = 28.000\text{ MHz}$ ;  $f_2 = 28.001\text{ MHz}$ .

$P_L$ (W)	f (MHz)	$V_{DS}$ (V)	$I_{DQ}$ (A)	$G_p$ (dB)	$\eta_D$ (%)	$d_3$ (dB) (note 2)	$d_5$ (dB) (note 2)
20 to 150 (PEP)	28	28	1	> 17 typ. 19	> 35 typ. 40	< -30 typ. -34	< -30 typ. -40

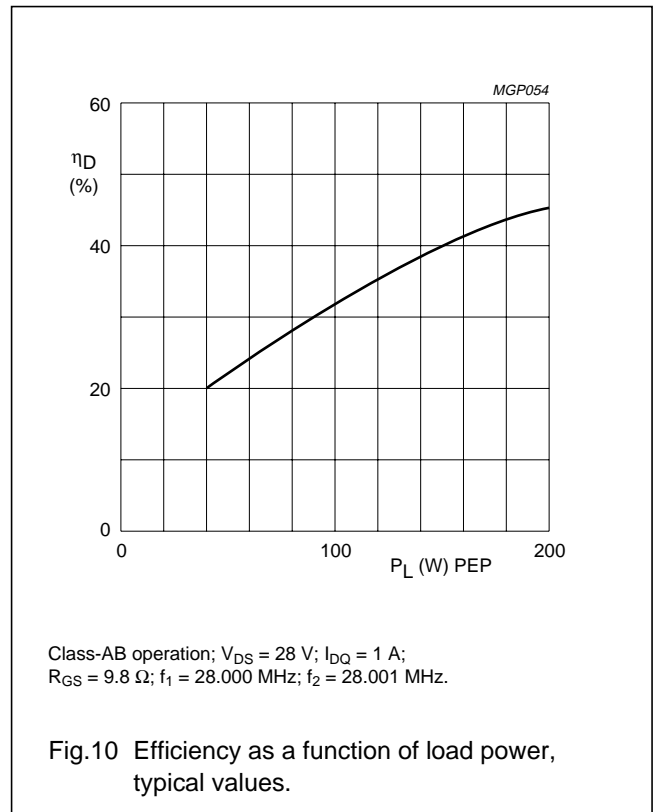
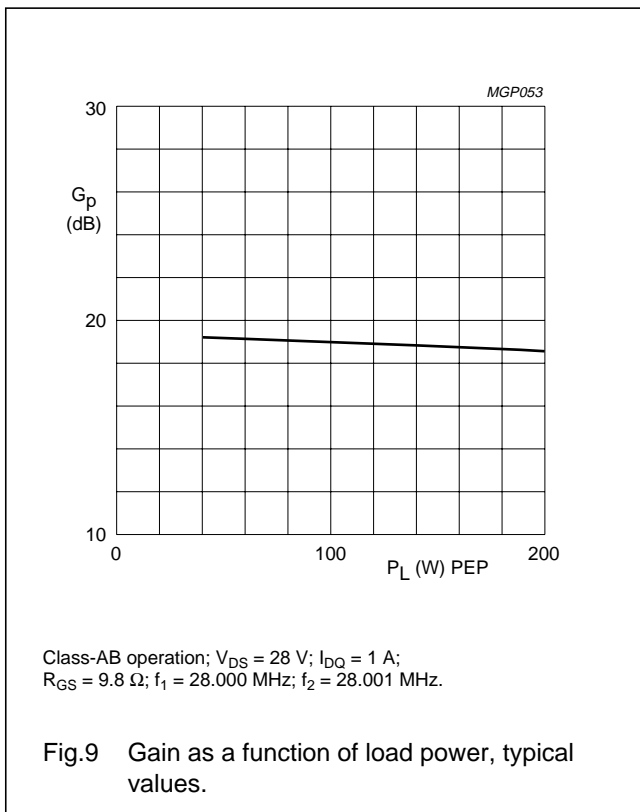
**Notes**

- Optimum load impedance:  $2.1 + j0\text{ }\Omega$ .
- Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

**Ruggedness in class-AB operation**

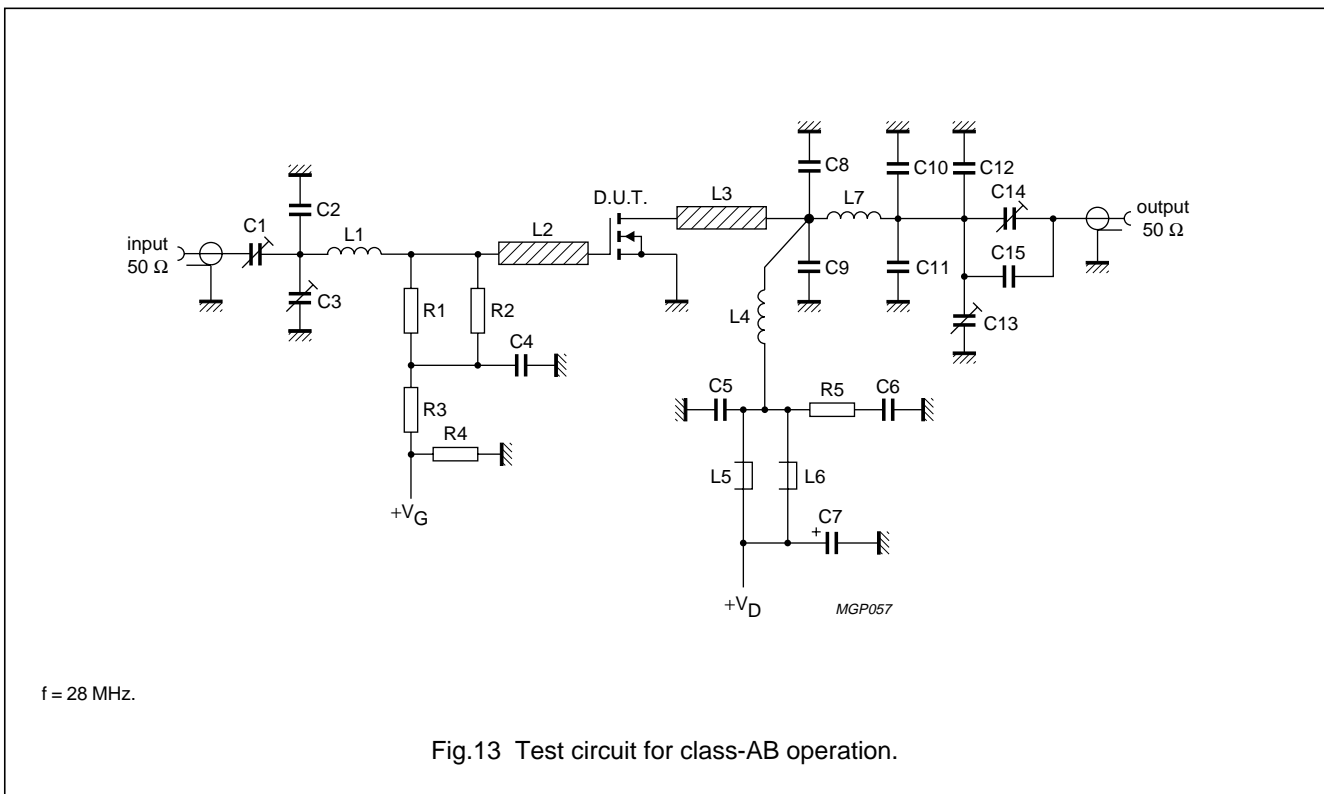
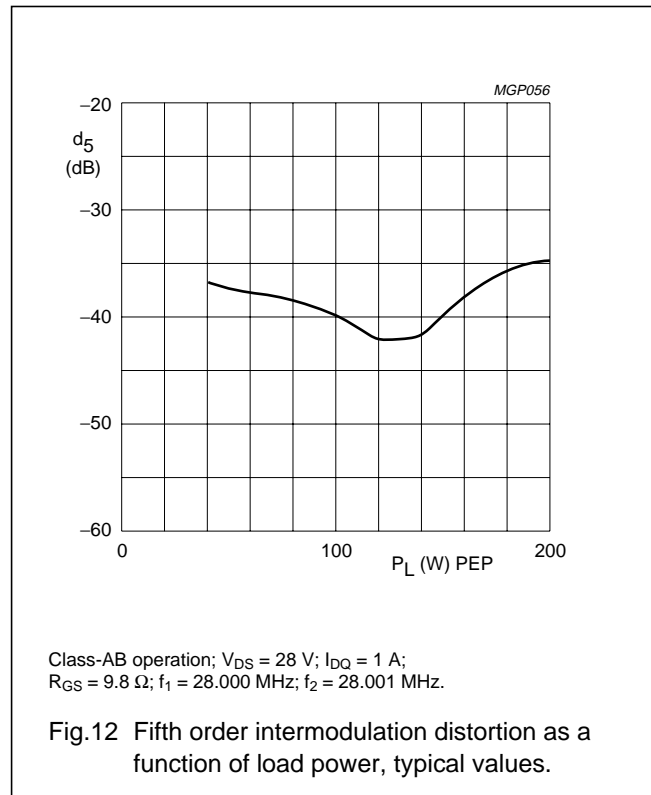
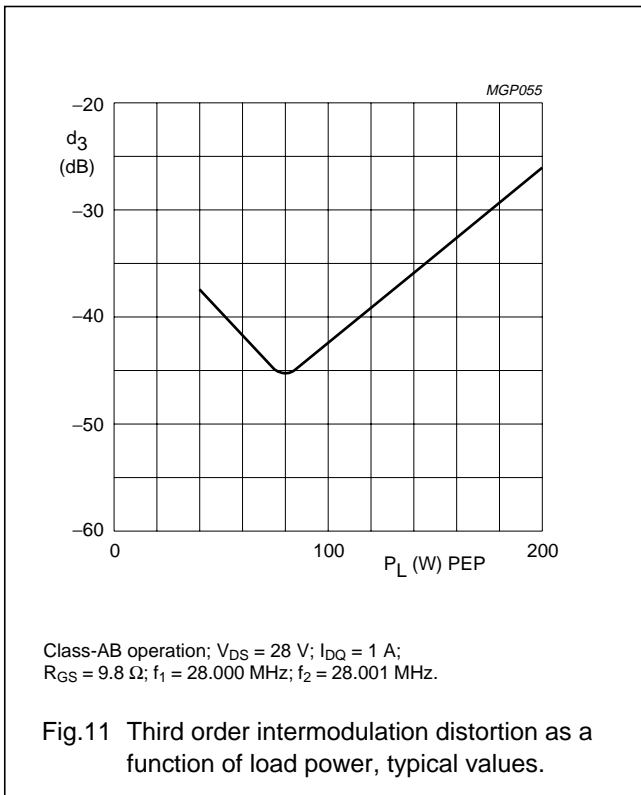
The BLF147 is capable of withstanding a load mismatch corresponding to  $V_{SWR} = 50$  through all phases under the following conditions:

$V_{DS} = 28\text{ V}$ ;  $f = 28\text{ MHz}$  at rated load power.



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## List of components (class-AB test circuit)

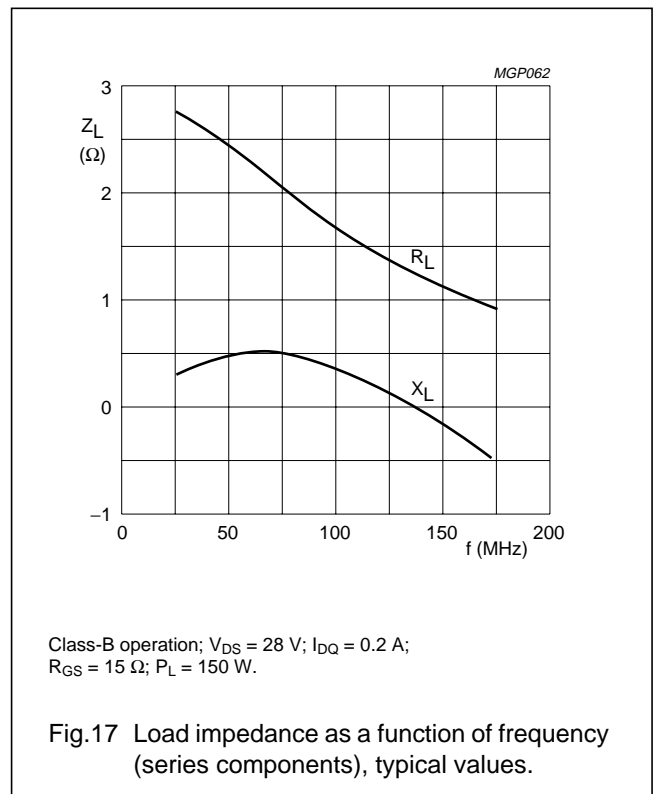
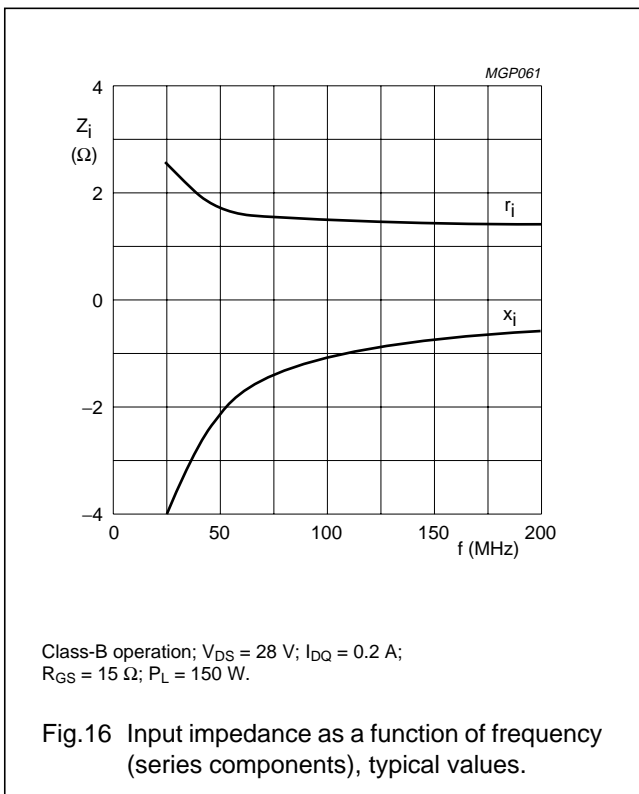
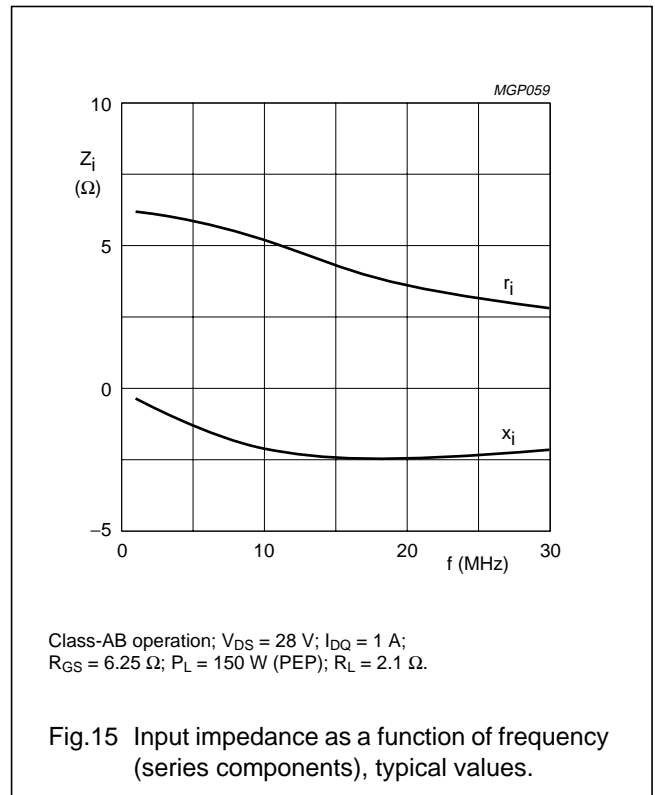
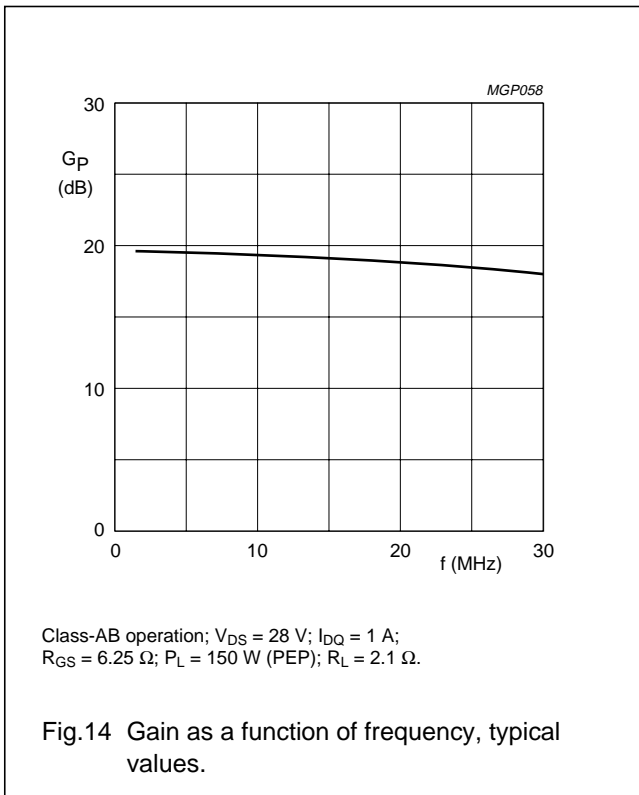
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C8, C9	multilayer ceramic chip capacitor (note 1)	75 pF		
C4, C5	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C6	multilayer ceramic chip capacitors in parallel	3 × 100 nF		2222 852 47104
C7	electrolytic capacitor	2.2 μF, 63 V		
C10	multilayer ceramic chip capacitor (note 1)	100 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	150 nF		
C15	multilayer ceramic chip capacitor (note 1)	240 pF		
L1	6 turns enamelled 0.7 mm copper wire	145 nH	length 5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 × 6 mm	
L4	4 turns enamelled 1.5 mm copper wire	148 nH	length 8 mm; int. dia. 10 mm; leads 2 × 5 mm	
L5, L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	3 turns enamelled 2.2 mm copper wire	79 nH	length 8 mm; int. dia. 8 mm; leads 2 × 5 mm	
R1, R2	1 W metal film resistor	19.6 Ω		2322 153 51969
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	1 MΩ		2322 151 71005
R5	1 W metal film resistor	10 Ω		2322 153 51009

## Notes

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ( $\epsilon_r = 2.2$ ), thickness 1.6 mm.

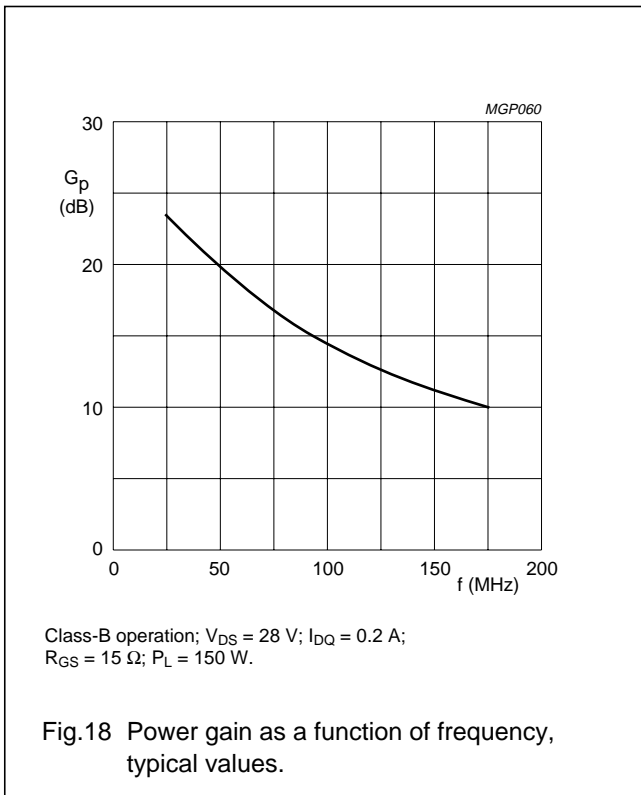
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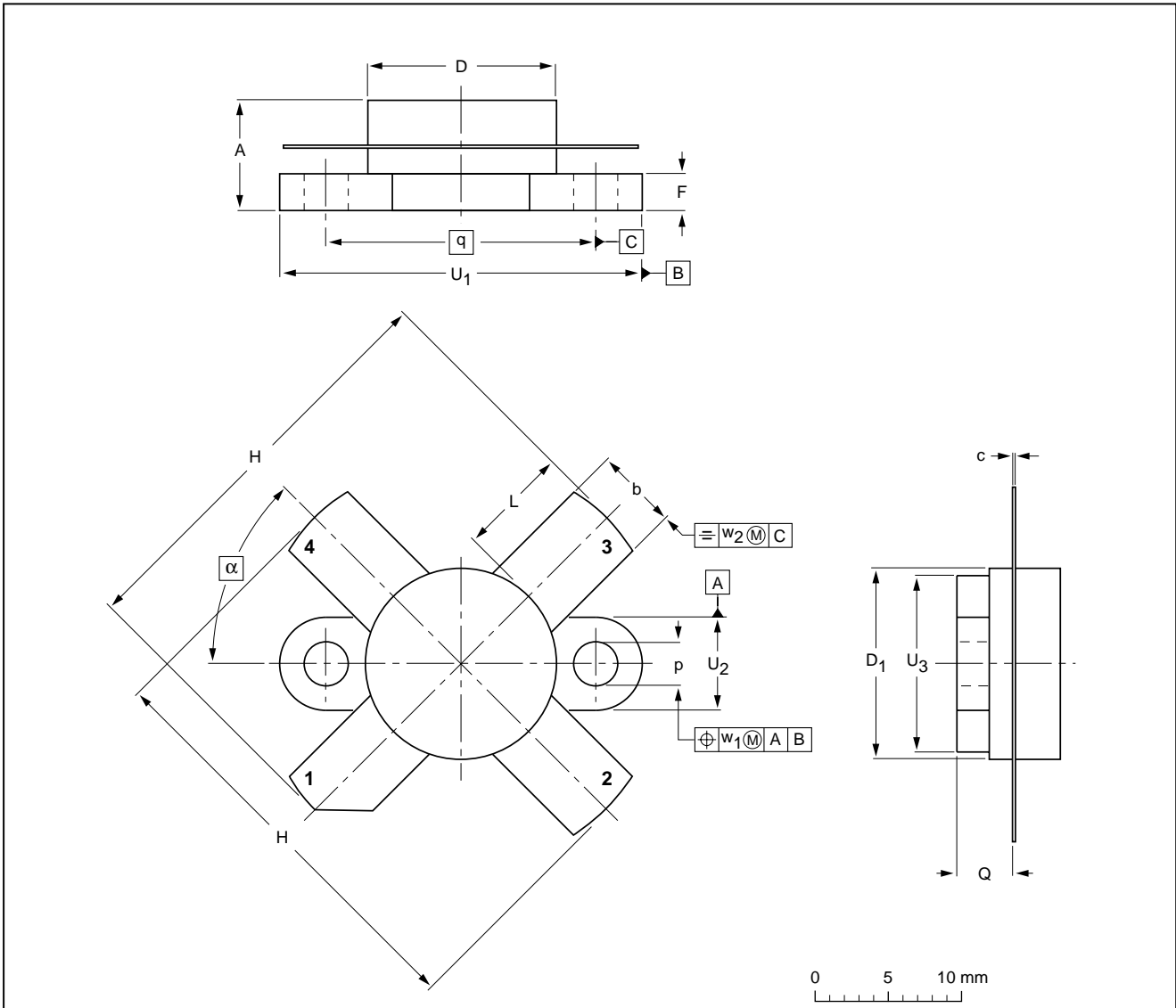
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PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT121B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	$\alpha$
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	7.93 6.32	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.51	1.02	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.312 0.249	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.02	0.04	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						97-06-28

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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